AMENDMENTS TO THE CLAIMS

1. (Original) A method of testing a memory die, comprising:

allowing said memory die to be placed in a location outside of a production facility of said die;

testing said memory die while said die is in said location; and

storing a partial memory cell address on said die as a result of said testing act, wherein said address corresponds to a memory cell having failed said testing act.

2. (Original) The method in claim 1, wherein said testing act comprises testing said die while said die is part of an electronic system.

3. (Original) The method in claim 2, wherein said testing act comprises testing said die while said electronic system is in a power management mode.

4. (Original) The method in claim 2, wherein said testing act comprises testing said die while said die is part of a computer system.

5. (Original) The method in claim 2, wherein said testing act comprises testing said die while said die is part of a telephone system.

6. (Original) The method in claim 5, wherein said testing act comprises testing said die while said die is part of a cellular telephone system.

7-57. (Canceled)

58. (New) A method of processing a plurality of memory circuits, comprising:

incorporating said plurality of memory circuits into an electronic system, said system having a primary function other than test or repair of said plurality of memory circuits; and

transmitting a signal in parallel to said plurality of memory circuits, said signal relating to a selection consisting of simultaneously testing said plurality of memory circuits and simultaneously repairing said plurality of memory circuits, said transmitting act occurring while said plurality of memory circuits are incorporated into said electronic system.

59. (New) The method in claim 58, wherein said transmitting act comprises transmitting a signal in parallel to a plurality of die, wherein each die of said plurality of die comprises at least one memory circuit.

60. (New) The method in claim 59, wherein said transmitting act comprises transmitting a signal to a module comprising said plurality of die.

61. (New) A method of processing of memory circuits, comprising:

incorporating said plurality of memory circuits into an electronic system, said system having a primary function other than test or repair of said plurality of memory circuits; and

transmitting a signal in parallel to said plurality of memory circuits, wherein said transmitting act further comprises programming at least one programmable device on at least one memory circuit of said plurality, and wherein said transmitting act occurs while said plurality of memory circuits are incorporated into said electronic system.

62. (New) The method in claim 61, wherein said transmitting act comprises repairing said at least one memory circuit.

63. (New) A method of processing a plurality of memory circuits, comprising:

incorporating said plurality of memory circuits into an electronic system, said system having a primary function other than test or repair of said plurality of memory circuits; and

transmitting a signal in parallel to said plurality of memory circuits, said signal relating to a selection consisting of simultaneously testing said plurality of memory circuits and simultaneously generating a programming voltage at each of said plurality of memory circuits, said transmitting act occurring while said plurality of memory circuits are incorporated into said electronic system.